Amendment to the Specification

Please amend the paragraph beginning on line 3 of page 10 as follows:

During stress, when C1 clock **160** is high (1), C2 clock **165** is low (0), VDD1 is high, VDD2 is low, all L1 latches **145** are powered and all L2 latches **150** are de-powered. Data in logic circuits **155B** is latched by L1 latches **145**. Data in logic circuits **155A** cannot be latched by L2 latches **150** since all the L2 latches are de-powered. Only L1 latches **145** and logic circuits **155A** are drawing current when C1 clock **160** is high.